

Fig. 1
PRIOR ART

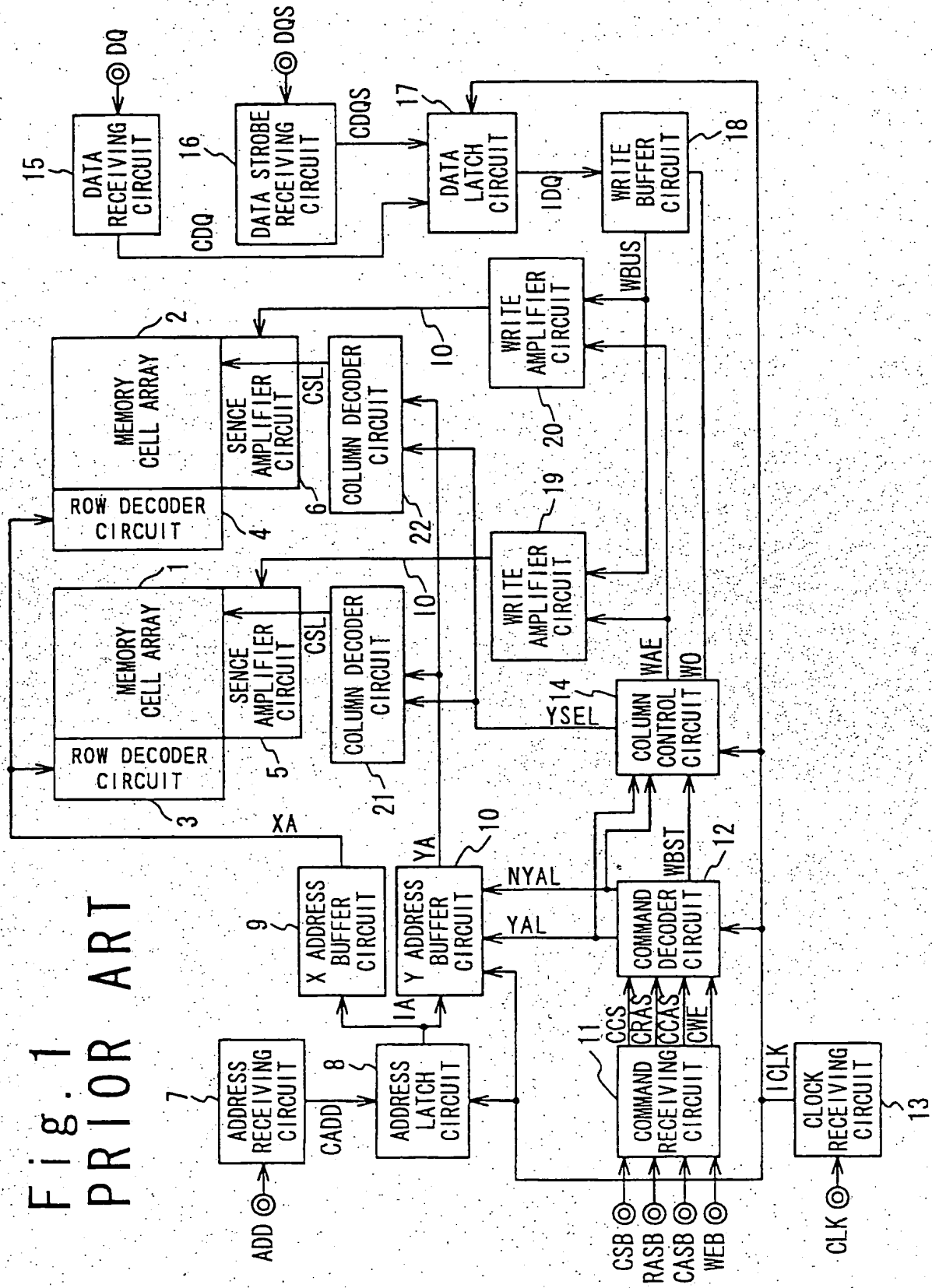


Fig. 2 PRIOR ART

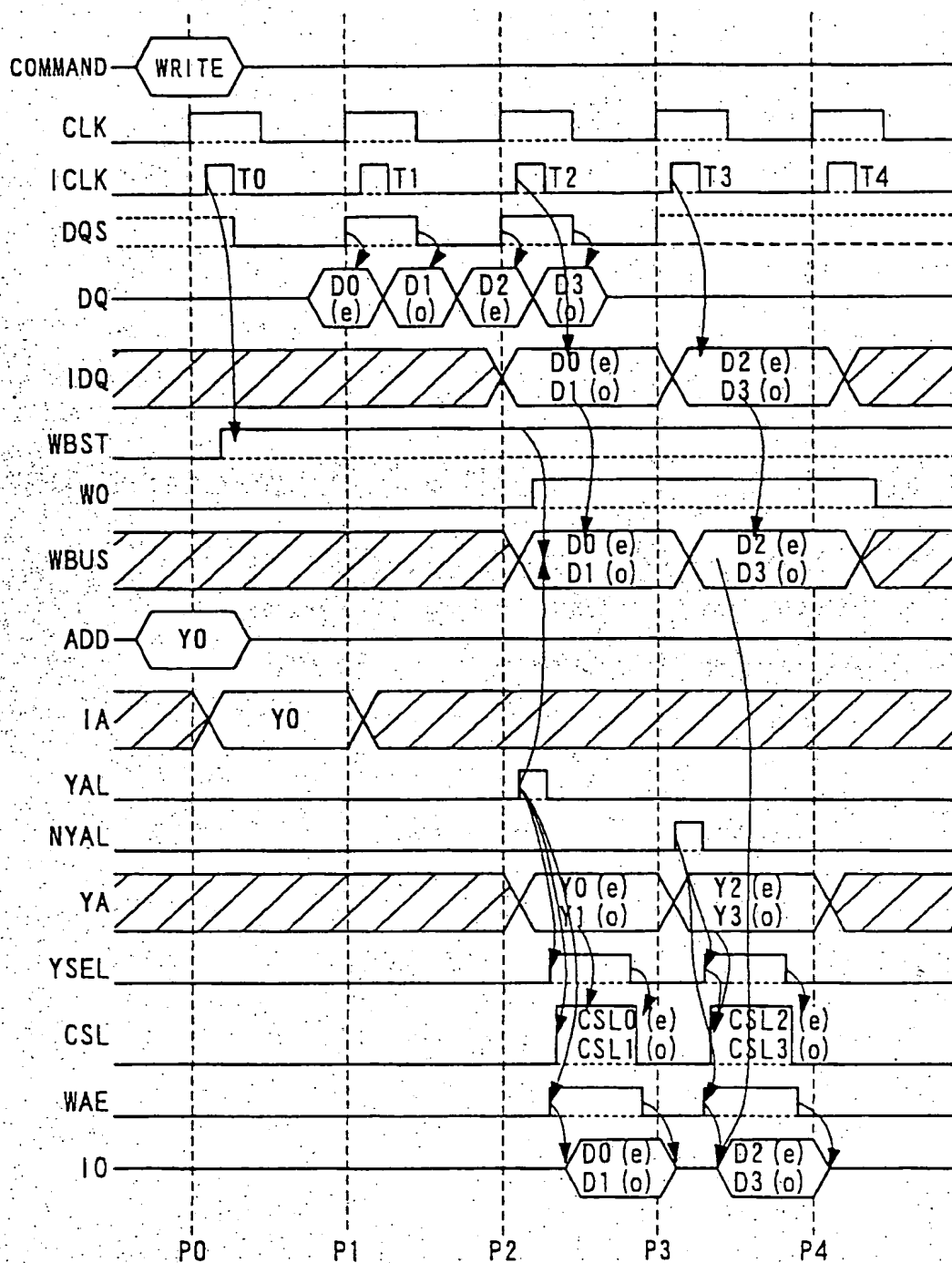


Fig. 3 PRIOR ART

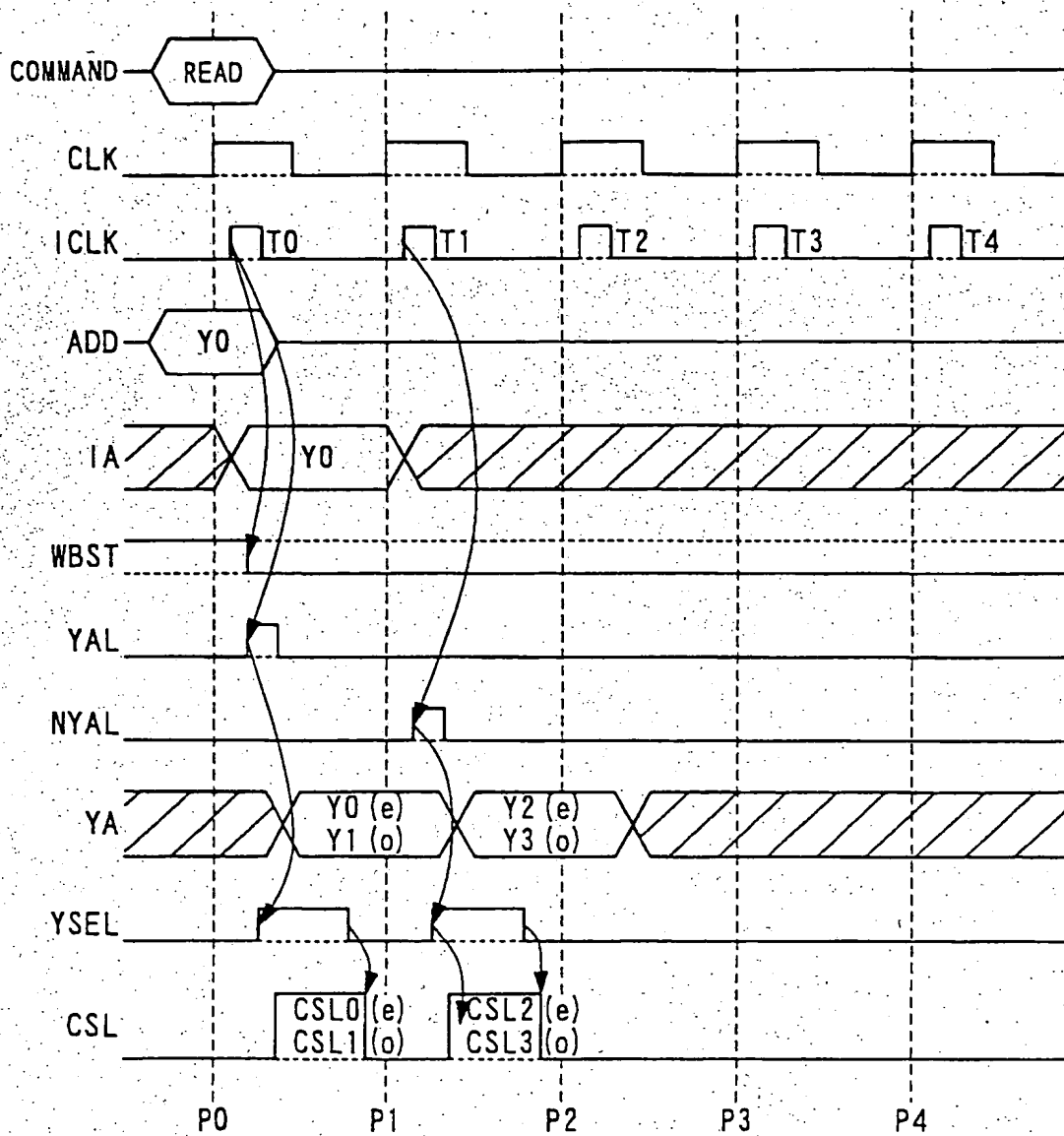


Fig. 4
PRIOR ART

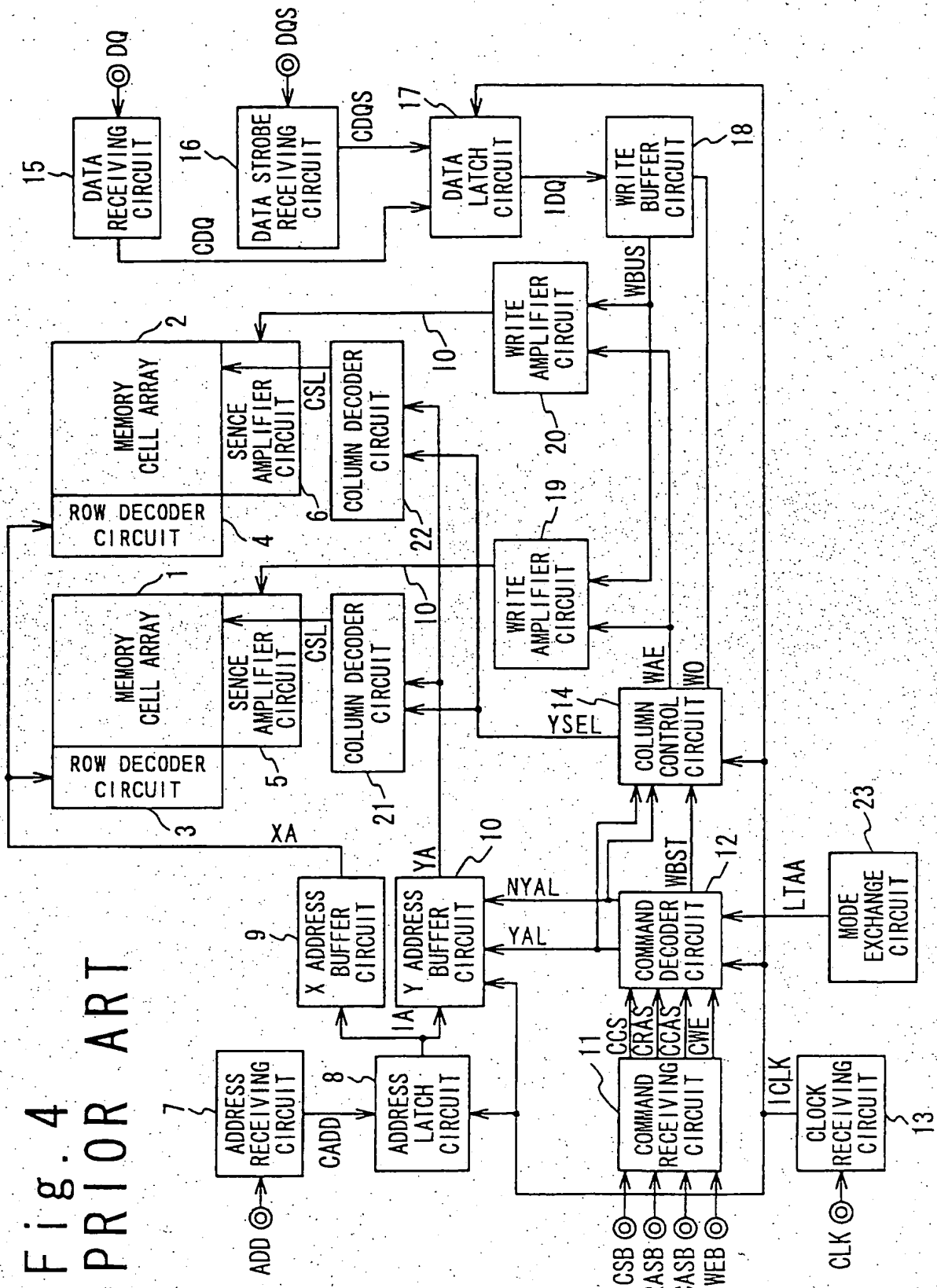


Fig. 5 PRIOR ART

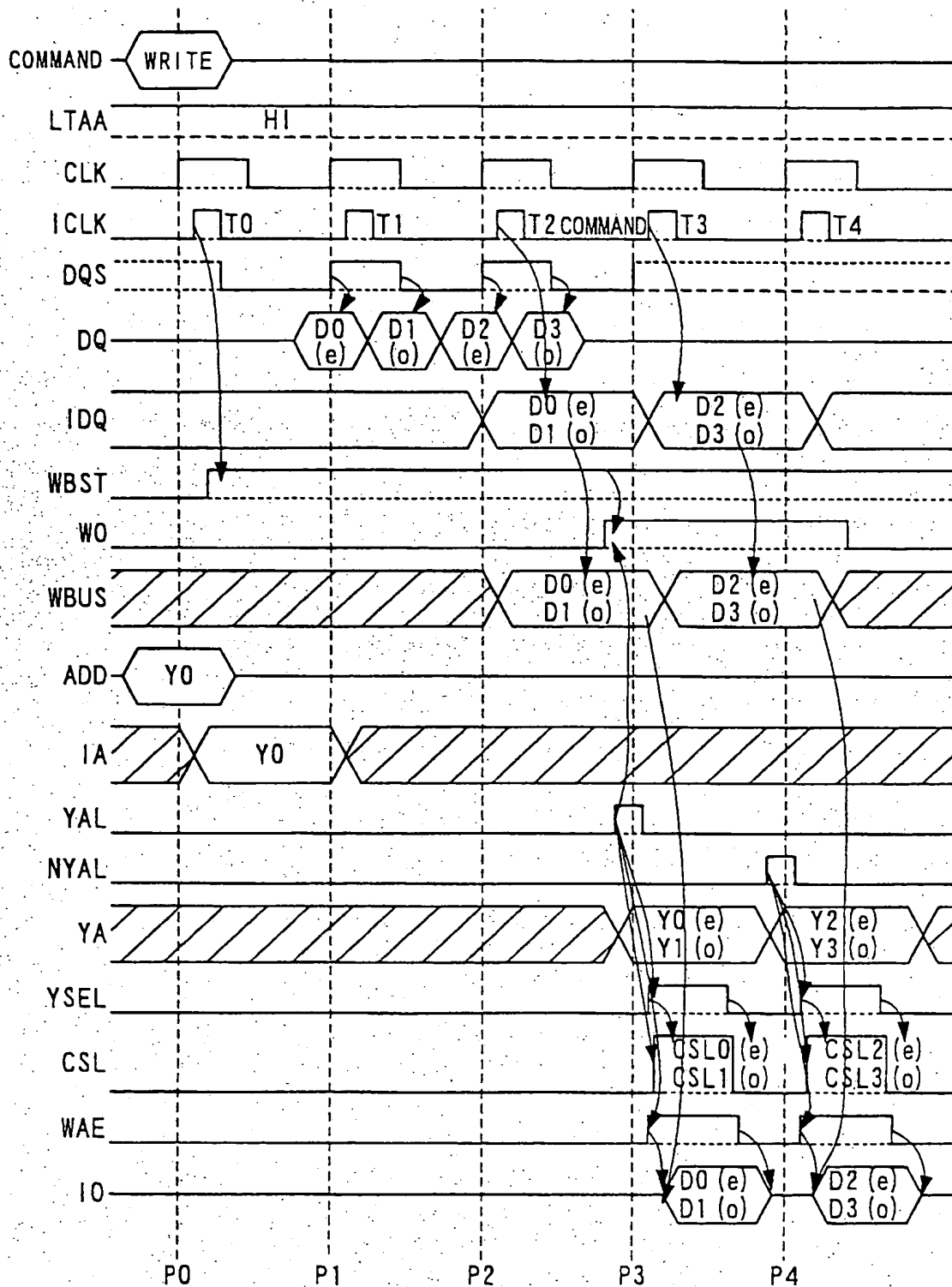
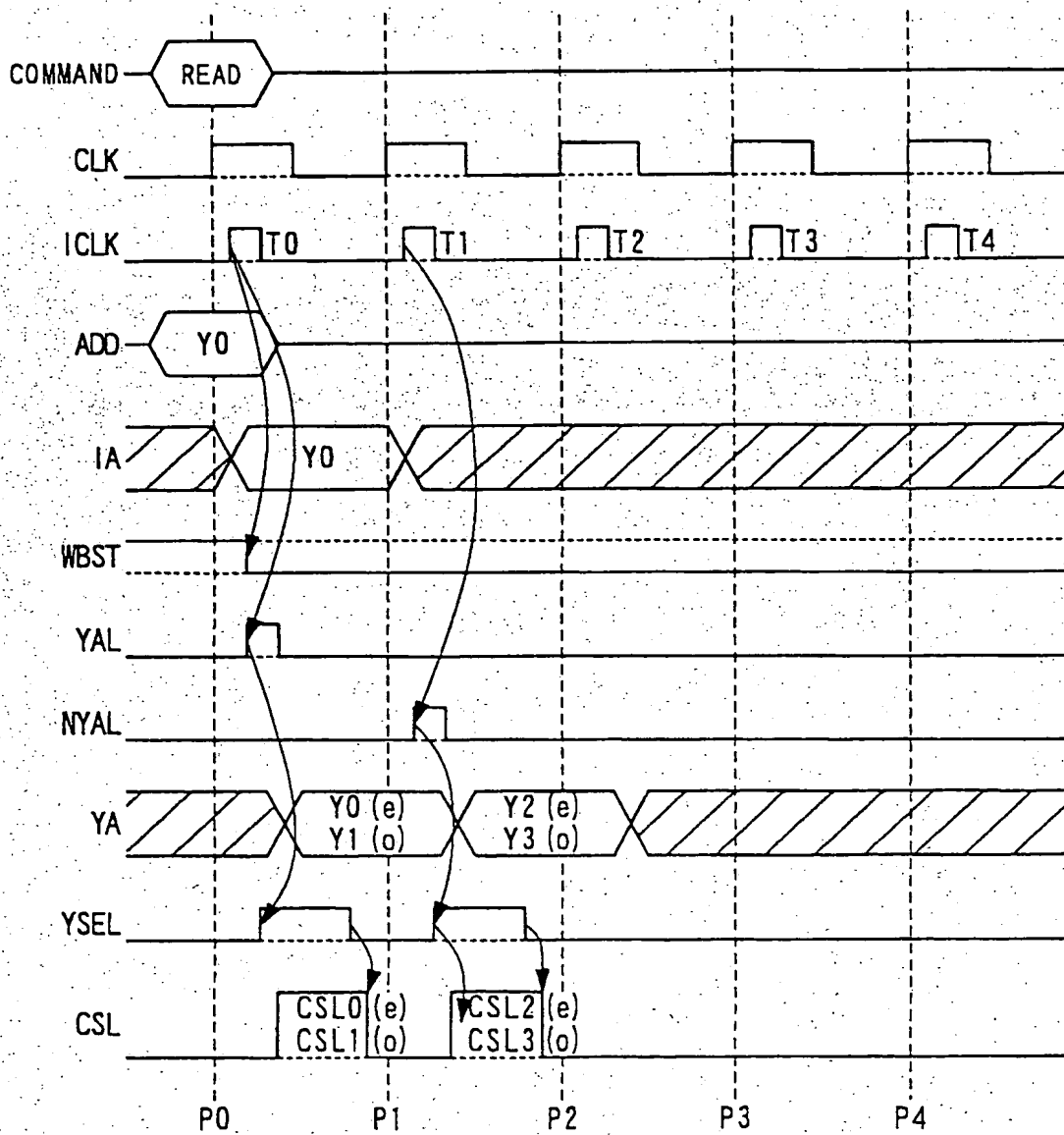


Fig. 6 PRIOR ART



The schematic diagram illustrates a control circuit 31 for a video signal processing system. The circuit is divided into two main sections, each containing a multiplexer and a delay circuit. The inputs to the control circuit 31 are CCS, CRAS, CCAS, CWE, and ICLK. The output of the control circuit 31 is YALO. The YALO signal is processed by a delay circuit 38, which outputs YALO. The YALO signal is also processed by a multiplexer 40, which outputs YAL. The YALO signal is also processed by a delay circuit 39, which outputs NYALO. The NYALO signal is processed by a multiplexer 50, which outputs NYAL. The circuit also includes a control circuit 31, a delay circuit 38, a delay circuit 39, a multiplexer 40, and a multiplexer 50. The circuit is labeled with various components and signals, including 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 50, 51, 52, 53, 54, 55, 56, 62, and 63.

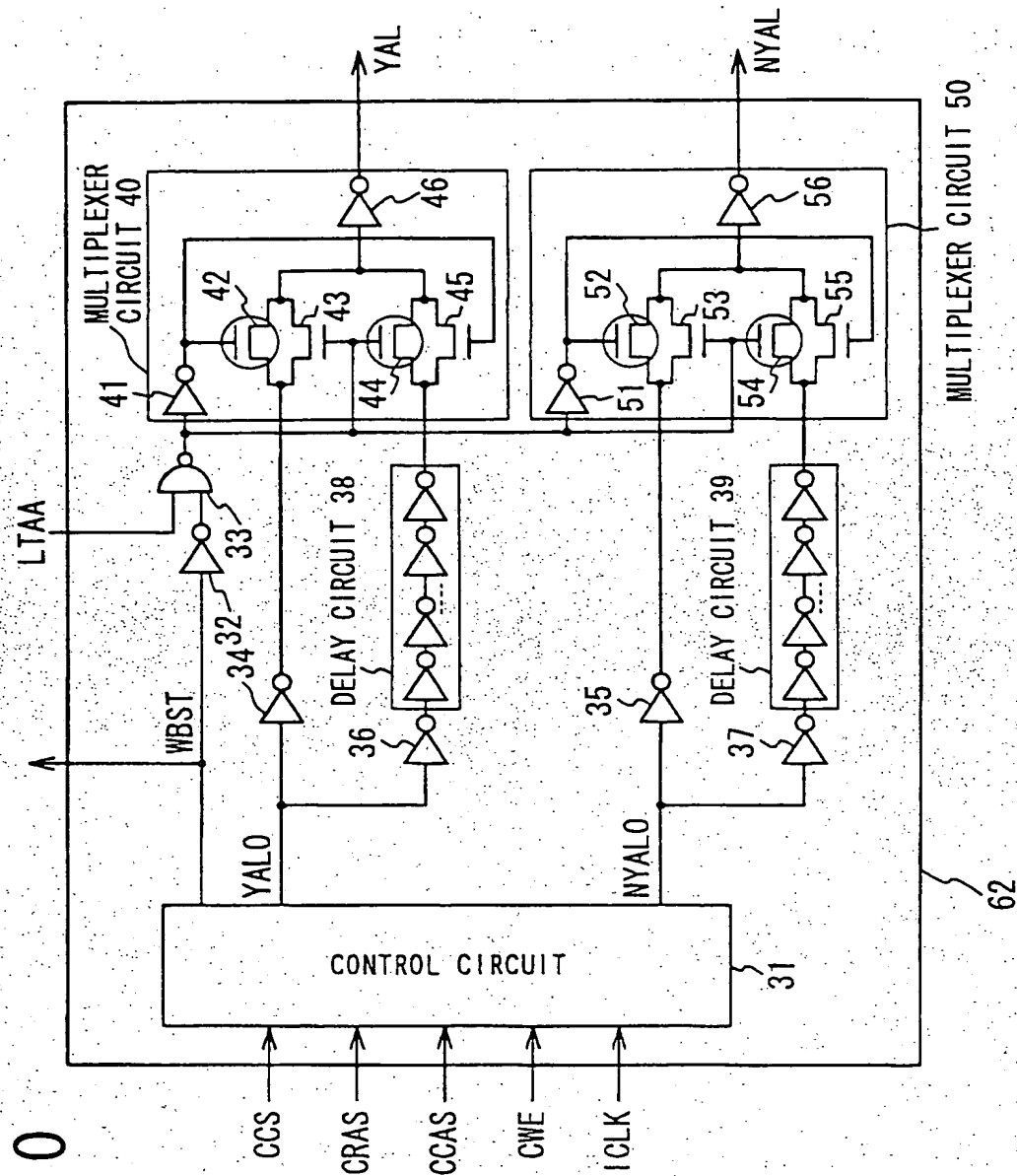


Fig. 9

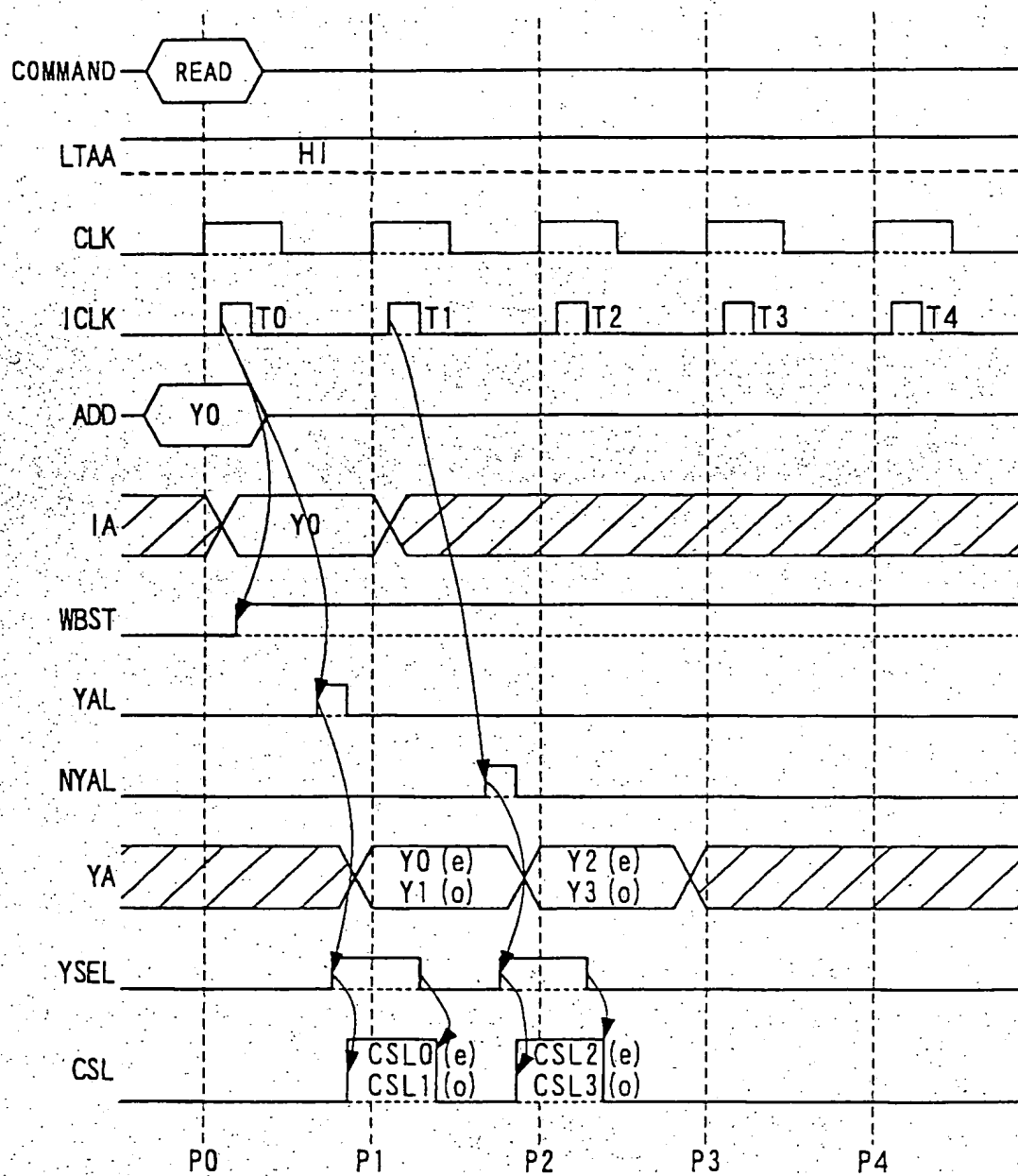


Fig. 8

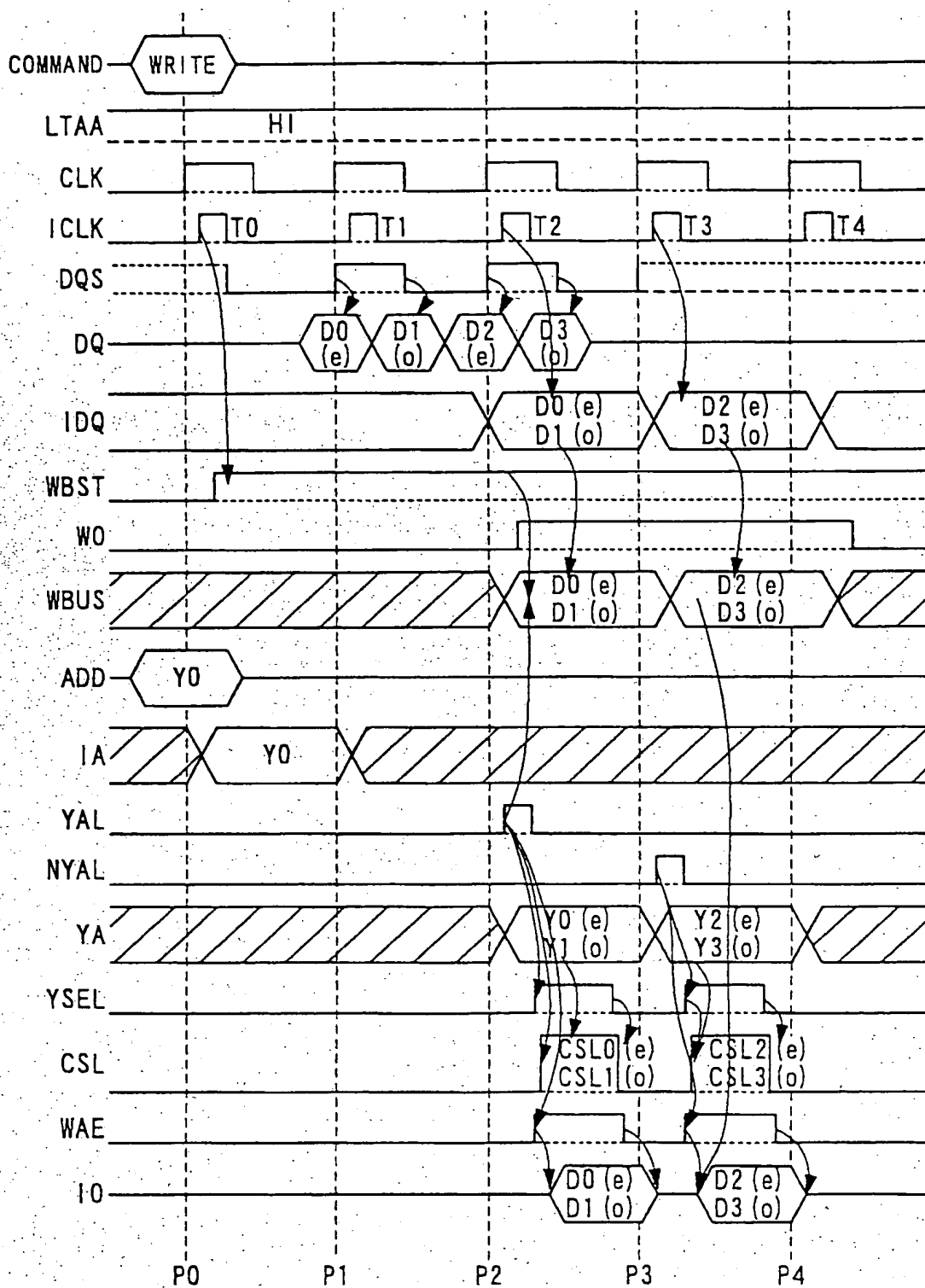


Fig. 7

The diagram illustrates a memory system architecture with the following components and connections:

- Input/Output Signals:** ADD, CADD, CDQ, DQ, DQS, CSB, CRASB, CASB, WEB, CLK, LTAA, WAE, WSEL, WBUS, IDQ, WOE.
- Control and Addressing:**
 - ADDRESS RECEIVING CIRCUIT (7)** receives ADD and outputs CADD to the **ADDRESS LATCH CIRCUIT (8)**.
 - ADDRESS LATCH CIRCUIT (8)** outputs IA to the **X ADDRESS BUFFER CIRCUIT (9)** and **Y ADDRESS BUFFER CIRCUIT (10)**.
 - COMMAND RECEIVING CIRCUIT (11)** receives CSB, CRASB, CASB, and WEB, and outputs CCS, CRAS, CCAS, and CWE to the **COMMAND DECODER CIRCUIT (62)**.
 - COMMAND DECODER CIRCUIT (62)** outputs WAE, WSEL, and WOE to the **COLUMN CONTROL CIRCUIT (14)**.
 - MODE EXCHANGE CIRCUIT (23)** receives LTAA and outputs WAE, WSEL, and WOE to the **COLUMN CONTROL CIRCUIT (14)**.
- Memory Arrays and Decoding:**
 - MEMORY CELL ARRAY (1)** and **MEMORY CELL ARRAY (2)** are connected to **ROW DECODER CIRCUIT (3)** and **ROW DECODER CIRCUIT (4)** respectively.
 - SENCE AMPLIFIER CIRCUIT (5)** and **SENCE AMPLIFIER CIRCUIT (6)** are connected to the memory arrays and output CSL to the **COLUMN DECODER CIRCUIT (21)** and **COLUMN DECODER CIRCUIT (10)** respectively.
 - COLUMN DECODER CIRCUIT (21)** outputs YA to the **Y ADDRESS BUFFER CIRCUIT (10)**.
 - COLUMN DECODER CIRCUIT (10)** outputs NYAL to the **Y ADDRESS BUFFER CIRCUIT (10)**.
- Data Path and Latching:**
 - DATA RECEIVING CIRCUIT (15)** receives CDQ and outputs IDQ to the **DATA LATCH CIRCUIT (17)**.
 - DATA STROBE RECEIVING CIRCUIT (16)** receives DQS and outputs IDQ to the **DATA LATCH CIRCUIT (17)**.
 - DATA LATCH CIRCUIT (17)** outputs IDQ to the **WRITE BUFFER CIRCUIT (18)**.
 - WRITE BUFFER CIRCUIT (18)** outputs WBUS to the **WRITE AMPLIFIER CIRCUIT (19)** and **WRITE AMPLIFIER CIRCUIT (20)**.
 - WRITE AMPLIFIER CIRCUIT (19)** and **WRITE AMPLIFIER CIRCUIT (20)** output WAE, WSEL, and WOE to the **COLUMN CONTROL CIRCUIT (14)**.

